REMARKS

Claims 1-61 are pending in the application, and claims 25-36 and 55-61 are withdrawn. The Applicants' attorney has amended claims 1-3, 5-10, 12-13, 15, 18-20, 22-23, 37, 45, 51, and 53, and has cancelled claim 16 without prejudice or disclaimer. As discussed below, all of the claims are in condition for allowance. **But if after considering this response the Examiner does not allow all of the claims, then the Applicants' attorney requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Objections To The Specification

The Applicants' attorney has amended the title to overcome this objection, and thus requests the Examiner to withdraw this objection.

Objections To The Drawings

The Examiner is mistaken that reference number "58" was deleted from paragraph [50] of FIG. 3 in the response to the first office action. Therefore, "58" is in the drawings (FIG. 3) and in the written description (paragraph [50]). Consequently, because this objection is improper, the Applicants' attorney requests the Examiner to withdraw it.

Rejection Of Claims 1-3, 5-6, 9-12, and 14-17 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 6,108,693 To Tamura

Claim 1

Claim 1 as amended recites a processor operable to publish data and to load the published data into first and second parallel buffers.

For example, referring, *e.g.*, to FIGS. 3-5 and paragraphs [67] – [72] and [83] of the patent application, in an embodiment, a processor 42 is operable, under the control

of an application thread 100_3, to publish data, and is operable, under the control of data-transfer objects 86_{3a} and 86_{5a}, to load the published data into first and second parallel buffers 106_3 and 106_5, respectively. A data-transfer object 86_{3b} retrieves the data from the buffer 106_3 and packages the data into a first message for transmission to a first destination. Similarly, a data-transfer object 86_{5b} retrieves the data from the buffer 106_5 and packages the data into a second message for transmission to a second destination.

In contrast, Tamura does not disclose a processor operable to publish data and to load the published data into first and second parallel buffers. Referring, *e.g.*, to Tamura's FIG. 4, even if the first and second buffers 442a are parallel buffers, the transmitting processor 410 is operable only to load data from the array A into one or the other of the buffers 442a, but not into both of these buffers (see also FIG. 6). Furthermore, even if the array A is a buffer, it is not parallel to the first or second buffer 442a. To load data into one of the first and second buffers 442a, the transmitting processor 410 must first load the data into the array A, and then transfer the data from the array A into the one buffer 442a. Therefore, the array A is serial, not parallel, to each of the buffers 442a.

Claims 2-3, 5-6, and 9

These claims are patentable by virtue of their respective dependencies from claim 1.

Claim 10

Claim 10 as amended recites a processor operable to generate data under the control of an application, load the data into a buffer, unload the data from the buffer, and process the unloaded data under the control of the application.

For example, referring, e.g., to FIGS. 3-5 and paragraph [82] of the patent application, in an embodiment, a processor 42 is operable to generate data under the control of a first thread 100_3 of an application 80, load the data into a buffer 106_5 under the control of a data-transfer object 86_{5a}, unload the data from the buffer 106_5 under the

control of a second data-transfer object 86_{5b}, and process the unloaded data under the control of a second thread 100_4 of the application 80.

In contrast, Tamura does not disclose a processor operable to generate data under the control of an application, load the data into a buffer, unload the data from the buffer, and process the unloaded data under the control of the application. Referring, e.g., to Tamura's FIG. 4, Tamura includes a processor 410 operable to execute a transmitting program 400. But even if the processor 410 generates data under the control of the program 400 and loads the data into the first or second buffer 442a, the processor 410 does not unload the data from the buffer 442a, and does not process the unloaded data under the control of the program 400. Instead, it is the receiving processor 420 that unloads the data and that processes the unloaded data under the control of a different program 430. Therefore, at the very least, Tamura does not generate and process data with the same program.

Claims 11-12 and 14-17

These claims are patentable by virtue of their respective dependencies from claim 10.

Rejection Of Claims 37, 39-43, 45, and 47-49 Under 35 U.S.C. § 102(b) As Being Anticipated By U.S. Patent 5,377,333 To Nakagoshi

Claim 37

Claim 37 as amended recites publishing with an application data that includes no information indicating a destination of the data, loading the published data into a buffer, retrieving the published data from the buffer, generating a message header that includes a destination of the retrieved data, and generating a message that includes the retrieved data and the message header.

For example, referring, *e.g.*, to FIG. 5 and paragraphs [67] – [69] of the patent application, in an embodiment, an application thread 100_1 publishes data that includes

no information indicating a destination of the data, a data-transfer object 86_{1a} loads the published data into a buffer 106_1, and a data-transfer object 86_{1b} retrieves the data from the buffer 106_1, generates a message header that includes a destination of the data within a pipeline accelerator 44 (FIG. 3), and generates a message that includes the retrieved data and the message header.

In contrast, Nakagoshi does not disclose loading into a buffer or retrieving from a buffer data that includes no information indicating a destination of the data. Referring to FIG. 9 and col. 11, lines 1-14, Nakagoshi discloses FIFO's 901 that store messages. But referring to FIG. 5 and col. 7, lines 39-53, Nakagoshi's messages include a transfer data receiving address 505, which is information indicating the destination of data 507.

Claims 39-43

These claims are patentable by virtue of their respective dependencies from claim 37.

Claim 45

Claim 45 as amended recites loading into a buffer data without a message header that indicates the destination of the data, the buffer corresponding to a destination of the data.

For example, referring, e.g., to FIGS. 3-5 and paragraphs [76] – [77], in an embodiment, a communication object 88 receives from a pipeline accelerator 44 a message that includes data and a header that indicates the destination (here the threads 100_1 and 100_2) of the data. A data-transfer object 86_{2b} loads into a buffer 106_2 the data from the message, but the data-transfer object does not load into the message header into the buffer 106_2. And the buffer 106_2 corresponds to the destination (here the threads 100_1 and 100_2) of the data.

In contrast, Nakagoshi does not disclose loading into a buffer received data without a message header that indicates the destination of the data, or that the buffer corresponds to the destination of the data. Referring to FIG. 9 and col. 11, lines 1-14, Nakagoshi discloses FIFO's 901 into which are loaded messages. But referring to FIG.

5 and col. 7, lines 39-53, Nakagoshi's messages include a message header that indicates the destination (the transfer data receiving address 505) of the data 507. Furthermore, referring e.g., to FIG. 1, each of Nakagoshi's exchangers 102 (which include the FIFO's 901) are arranged to pass data from any one cluster 103 to any other cluster 103; consequently, no FIFO 901 corresponds to the destination of data that is loaded into the FIFO. That is, one cannot predict the destination(s) of data within a FIFO 901 from the identity of the FIFO itself.

Claims 47-49

These claims are patentable by virtue of their respective dependencies from claim 45.

Rejection Of Claims 4 and 13 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tamura

Claim 4

This claim is patentable by virtue of its dependency from claim 1.

Claim 13

This claim is patentable by virtue of its dependency from claim 10.

Rejection Of Claim 7 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tamura In View Of U.S. 5,283,883 To Mishler

Claim 7

This claim is patentable by virtue of its dependency from claim 1.

Rejection Of Claims 8 and 18 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tamura In View Of The "Microsoft Computer Dictionary"

Claim 8

This claim is patentable by virtue of its dependency from claim 1.

Claims 18

This claim is patentable by virtue of its dependency from claim 10.

Rejection Of Claims 19-24 And 51 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tamura In View Of U.S. 5,909,565 To Morikawa

Claim 19

Claim 19 as amended recites a processor operable to construct a message including data retrieved from a buffer and information indicating a destination of the retrieved data and driving the message onto a bus, and a pipeline accelerator operable to receive the message from the bus, to recover the data from the message, and to process the recovered data without executing a program instruction.

For example, referring, e.g., to FIGS. 3-5 and paragraphs [67] – [72], in an embodiment, a processor 42, under control of a data-transfer object 861b, retrieves data from a buffer 1061, and under control of a communication object 88, constructs a message that includes the data from the buffer and information indicating a destination of the retrieved data within a pipeline accelerator 44, and drives the message onto a bus 50. The accelerator 44 is operable to receive the message from the bus 50, to recover the data from the message, and to process the recovered data without executing a program instruction.

In contrast, neither Tamura nor Morikawa disclose the construction of a message that includes data retrieved from a buffer and information indicating a destination of the

data, the driving of the message onto a bus, or a pipeline accelerator operable to receive the message from the bus, to recover the data from the message, or to process the data without executing a program instruction.

Referring, *e.g.*, to FIG. 4, Tamara's processors 410 and 420 transfer data and information indicating a destination of the data (*e.g.*, addresses) separately via address and data busses, not via messages. Also, the processors 410 and 420 can process data only by executing instructions.

Similarly, referring, e.g., to FIG. 1, Morikawa's processors 101 and 102 do not transfer data via messages, and can process data only by executing instructions.

Therefore, the combination of Tamura and Morikawa does not disclose or suggest all of the limitations of claim 19.

Claims 20-21

These claims are patentable by virtue of their dependencies from claim 19.

Furthermore, regarding claim 20, neither Tamura nor Morikawa discloses a pipeline accelerator that includes a field-programmable gate array.

Claim 22

Claim 22 as amended recites a pipeline accelerator operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data, to package the data and header into a message, and to drive the message onto a bus.

Referring, *e.g.*, to FIGS. 3-5 and paragraphs [73] – [79] of the patent application, in an embodiment, a pipeline accelerator 44 is operable to generate data without executing a program instruction, to generate a header including information indicating a destination of the data (e.g., a thread 100), to package the data and header into a message, and to drive the message onto a bus 50.

In contrast, neither Tamura nor Morikawa disclose a pipeline accelerator operable to generate data without executing a program instruction, to generate a header

including information indicating a destination of the data, to package the data and header into a message, and to drive the message onto a bus.

Referring, e.g., to FIG. 4, Tamara's processors 410 and 420 transfer data and information indicating a destination of the data (e.g., addresses) separately via address and data busses, not via messages. Also, the processors 410 and 420 can process data only by executing instructions.

Similarly, referring, e.g., to FIG. 1, Morikawa's processors 101 and 102 do not transfer data via messages, and can process data only by executing instructions.

Therefore, the combination of Tamura and Morikawa does not disclose or suggest all of the limitations of claim 22.

Claims 23-24

These claims are patentable by virtue of their respective dependencies from claim 22.

Claim 51

Claim 51 as amended recites generating information that indicates a destination of data, packaging the retrieved data and the information into a message, driving the message onto a bus, receiving the message from the bus and processing the published data with a pipeline accelerator that includes a field-programmable gate array.

In contrast, referring, e.g., to FIG. 4, Tamara's processors 410 and 420 transfer data and information indicating a destination of the data (e.g., addresses) separately via address and data busses, not via messages. Also, the processors 410 and 420 do not include a field-programmable gate array.

Similarly, referring, e.g., to FIG. 1, Morikawa's processors 101 and 102 do not transfer data via messages, and do not include a field-programmable gate array.

Therefore, the combination of Tamura and Morikawa does not disclose or suggest all of the limitations of claim 51.

Rejection Of Claims 38, 44, 46, 50, and 53-54 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Nakagoshi

Claims 38 and 44

These claims are patentable by virtue of their dependencies from claim 37.

Claims 46 and 50

These claims are patentable by virtue of their dependencies from claim 45.

Claim 53

Claim 53 as amended recites loading into a buffer data absent a header that includes a destination of data, the buffer being identified by the destination.

For example, referring, e.g., to FIGS. 3-5 and paragraphs [76] – [77], in an embodiment, a communication object 88 receives from a pipeline accelerator 44 a message that includes data and a header that indicates the destination (here the threads 100_1 and 100_2) of the data. A data-transfer object 86_{2b} loads into a buffer 106_2 the data from the message, but the data-transfer object does not load the message header into the buffer 106_2. And the buffer 106_2 is identified by the destination (here the threads 100_1 and 100_2) of the data.

In contrast, Nakagoshi does not disclose or suggest loading into a buffer received data absent a message header that includes the destination of the data, or that the buffer is identified by the destination of the data. Referring to FIG. 9 and col. 11, lines 1-14, Nakagoshi discloses FIFO's 901 into which are loaded messages. But referring to FIG. 5 and col. 7, lines 39-53, Nakagoshi's messages include a message header that indicates the destination (the transfer data receiving address 505) of the data 507. Furthermore, referring e.g., to FIG. 1, each of Nakagoshi's exchangers 102 (which include the FIFO's 901) are arranged to pass data from any one cluster 103 to any other cluster 103; consequently, no FIFO 901 is identified by the destination of data that is loaded into the FIFO.

Claim 54

Claim 54 is patentable by virtue of its dependency from claim 53.

Rejection Of Claim 52 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Tamura In View Of Morikawa In Further View Of Microsoft

Claim 52

Claim 52 is patentable by virtue of its dependency from claim 51.

CONCLUSION

In view of the foregoing, claims 4, 11, 14, 17, 21, 24, 38-44, 46-50, 52, and 54 as previously pending and claims 1-3, 5-10, 12-13, 15, 18-20, 22-23, 37, 45, 51, and 53 as amended are in condition for allowance. Therefore, the issuance of a formal Notice of Allowance at an early date is respectfully requested. **If the Examiner does not agree that all claims are in condition for allowance, the Examiner is respectfully requested to telephone the undersigned prior to issuing an action rejecting the claims to schedule a telephone interview.**

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 50-1464.

If the Examiner believes that a phone interview would be helpful, he is respectfully requested to contact the Applicant's attorney, Bryan Santarelli, at (425) 455-5575.

DATED this 19th Day of December, 2007.

Respectfully submitted,

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